REMARKS

In the Office Action, claims 4-10,12-13,43-45,48-49,51-64, and 88-96 were rejected under §102(e) as being unpatentable over United States Patent 6,301,686 issued to Kikuchi et al. ("Kikuchi"). Furthermore, claims 11, 46-47, 50 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In this Amendment, Applicants have amended claims 4, 43, 58, 60, 61 and 88 but have not added or canceled any claims. Accordingly, claims 4-13, 43-64, 88-96 remain pending in the application after entry of this Amendment.

I. Rejection of claims 4-10 and 12-13 under § 102(e)

Claims 4-10 and 12-13 were rejected under § 102(e) as being unpatentable over Kikuchi. Claims 5-10 and 12-13 are dependent directly or indirectly on independent claim 4. Claim 4 recites in part, a method that places circuit modules in an integrated circuit ("IC") layout. The IC layout has a number of circuit elements. The IC layout has a net that has a set of circuit elements. The method uses a diagonal line to measure a placement metric. The method measures the placement metric by calculating an estimate of the length of interconnect lines necessary to connect the circuit elements of the net during a routing operation. The calculation measures the length of at least one line that is at least partially diagonal.

Applicants respectfully submit that Kikuchi does not disclose, teach, or even suggest such a method. For instance, Applicants respectfully submit that Kikuchi does not disclose, teach or even suggest an IC placement method that measures a placement metric by measuring the

length of one line that is at least partially diagonal to calculate an estimate of the length of interconnect lines necessary to connect the circuit elements of the net during a routing operation.

Kikuchi describes a graphic layout compaction system that calculates a capacity area. Within the capacity area, a first component can move in any direction towards a second component in consideration of a capacity between the edges of the components. The capacity is obtained by adding a necessary space to a width of particular routes put between a first component and a second component. A component compactor then moves the first component towards the second component such that the first component does not interfered with the capacity area. Next, a rerouting unit shapes the particular routes into shaped particular routes having configurations including oblique parts to reroute the shaped particular routes in a space between the first and the second components (Column 4, lines 16-31).

The Examiner cites column 1, lines 23-38 and column 10, lines 55-67 as disclosing the method of claim 4. The cited sections describe a graphic compaction system that obtains a distance between two components in order to determine the capacity between the edges of the components. These two components are not even necessarily two components on the same net.

In contrast, claim 4 recites a method that **measures a placement metric** by calculating an estimate of the length of interconnect lines necessary to connect the **circuit elements of a net during a routing operation**. This calculation measures the length of at least one line that is at least partially diagonal. Kikuchi does not disclose, teach, or even suggest such a limitation.

Accordingly, Applicants respectfully submit that Kikuchi does not render claim 4 unpatentable. As Claims 5-10 and 12-13 are dependent on claim 4, Applicants respectfully submit that claims 5-10 and 12-13 are patentable over Kikuchi for at least the same reasons that were discussed above for claim 4.

In view of the foregoing, Applicants respectfully request reconsideration and withdrawal of the § 102(e) rejection of claims 4-10 and 12-13.

II. Rejection of claims 43-45, 48-49, 51-57 under § 102(e)

Claims 43-45, 49, 51-57 were rejected under § 102(e) as being unpatentable over Kikuchi. Claims 44-45, 48-49 and 51-57 are dependent directly or indirectly on independent claim 43. Claim 43 recites a method that places circuit modules in an integrated circuit ("IC") layout. The IC layout includes a net that has a plurality of circuit elements. The method constructs a connection graph that connects the circuit elements of the net. The connection graph has edges. At least one of the edges is at least partially diagonal. The method identifies a placement metric based on the connection graph. The method uses the placement metric to identify a placement of the circuit modules.

Applicants respectfully submit that Kikuchi does not disclose, teach, or even suggest such a method. For instance, Applicants respectfully submit that Kikuchi does not disclose, teach or even suggest a method that:

- constructs a connection graph that connects the circuit elements of the net, where the connection graph has edges and where at least one of the edges is at least partially diagonal;
- identifies a placement metric based on the connection graph; and
- uses the placement metric to identify a placement of circuit modules.

The Examiner rejects claim 43 on the basis of being similar manner as claim 4. As discussed above, Kikuchi describes a method that obtains a distance between two components (that are not necessarily part of the same net) in order to determine the capacity between the

edges of the components. In contrast, claim 43 recites in part, a method that (1) identifies a placement metric based on a net's connection graph with an edge that is at least partially diagonal, and then uses (2) the placement metric to identify a placement of the circuit modules. Nowhere in Kikuchi are such limitations disclosed, taught, or even suggested.

Accordingly, Applicants respectfully submit that Kikuchi does not render claim 43 unpatentable. As Claims 44-45, 48-49 and 51-57 are dependent on claim 43, Applicants respectfully submit that claims 44-45, 48-49 and 51-57 are patentable over Kikuchi for at least the same reasons that were discussed above for claim 43.

In view of the foregoing, Applicants respectfully request reconsideration and withdrawal of the § 102(e) rejection of claims 43, 45, 49 and 51-57.

III. Rejection of claims 58-60 under § 102(e)

Claims 58-60 were rejected under § 102(e) as being unpatentable over Kikuchi. Claims 59-60 are dependent directly or indirectly on independent claim 58. Claim 58 recites for an electronic design automation ("EDA") application, a method that places circuit modules in an integrated circuit ("IC") layout. The IC layout includes a plurality of nets each of which includes a plurality of circuit elements in the IC layout. The EDA application includes a wiring model that defines different types of interconnect lines for connecting the circuit elements of the nets. The wiring model has diagonal lines. The method, for each particular net, defines a minimum spanning tree that models the topology of interconnect lines for connecting the circuit elements of the particular net. The minimum spanning tree has edges. At least one of the edges of at least one of the minimum spanning trees is at least partially diagonal. The method calculates the length of the edges of the minimum spanning trees. The method combines the length calculations to obtain an

estimate of the total interconnect-line length needed for connecting the circuit elements of the nets during a routing operation. The method uses the combined length calculations to identify a placement of the circuit modules.

Applicants respectfully submit that Kikuchi does not disclose, teach, or even suggest such a method. For instance, Applicants respectfully submit that Kikuchi does not disclose, teach or even suggest a method that:

- for each particular net, defines a minimum spanning tree that models the topology of interconnect lines for connecting the circuit elements of the particular net, the minimum spanning tree having edges and where at least one of the edges of at least one of the minimum spanning trees is at least partially diagonal;
- calculates the length of the edges of the minimum spanning trees;
- combines the length calculations to obtain an estimate of the total interconnect-line length needed for connecting the circuit elements of the nets during a routing operation; and
- uses the combined length calculations to identify a placement of the circuit modules.

The Examiner identifies column 16, lines 22-38 and column 11, lines 1-18 of Kikuchi as disclosing the method of claim 58. Specifically, Examiner states that the comparison of the length of the third graph with two lengths of the above-mentioned two terminal graphs (column 11, lines 16-18) describes some of the limitations of the claim.

However, Kikuchi describes a comparison of the length of the third graph with two lengths of the above-mentioned two terminal graphs in order to determine whether the third graph is shorter than the length of the two terminal graphs. In contrast, claim 58 recites in part, a

placement method that (1) combines length calculations to **obtain an estimate** of the total interconnect-line length needed for connecting the circuit elements of the nets during a routing operation, and then (2) uses the combined length calculation to identify a placement of the circuit modules. Kikuchi does not disclose, teach, or even suggest such a method.

Accordingly, Applicants respectfully submit that Kikuchi does not render claim 58 unpatentable. As Claims 59-60 are dependent on claim 58, Applicants respectfully submit that claims 59-60 are patentable over Kikuchi for at least the same reasons that were discussed above for claim 58.

In view of the foregoing, Applicants respectfully request reconsideration and withdrawal of the § 102(e) rejection of claims 58-60.

IV. Rejection of claims 61-64 under § 102(e)

Claims 61-64 were rejected under § 102(e) as being unpatentable over Kikuchi. Claims 62-64 are dependent directly or indirectly on independent Claim 61. Claim 61 recites for an electronic design automation ("EDA") application, a method that places circuit modules in an integrated circuit ("IC") layout. The IC layout includes a plurality of nets each of which includes a plurality of circuit elements in the IC layout. The EDA application includes a wiring model that defines different types of interconnect lines for connecting the circuit elements of the nets. The wiring model has diagonal lines. The method, for each particular net, defines a Steiner tree that models the topology of interconnect lines for connecting the circuit elements of the particular net. The Steiner tree has edges. At least one of the edges of at least one of the Steiner trees is at least partially diagonal. The method calculates the length of the edges of the Steiner trees. The method combines the length calculations to obtain an estimate of the total interconnect-line length needed

for connecting the circuit elements of the nets during a routing operation. The method uses the combined length calculations to identify a placement of the circuit modules.

Applicants respectfully submit that Kikuchi does not disclose, teach, or even suggest such a method. For instance, Applicants respectfully submit that Kikuchi does not disclose, teach or even suggest a method that:

- for each particular net, defines a Steiner tree that models the topology of interconnect lines the circuit elements of the particular net, the Steiner tree having edges and where at least one of the edges of at least one of the Steiner trees is at least partially diagonal;
- calculates the length of the edges of the Steiner trees;
- combines the length calculations to obtain an estimate of the total interconnect-line length needed for connecting the circuit elements of the nets during a routing operation; and
- uses the combined length calculations to identify a placement of the circuit modules.

The Examiner identifies column 16, lines 22-38 and column 11, lines 1-18 of Kikuchi as disclosing the method of claim 61. However, as mentioned above, Kikuchi describes a comparison of the length of the third graph with two lengths of the above-mentioned two terminal graphs in order to determine whether the third graph is shorter than the length of the two terminal graphs. In contrast, claim 61 recites in part, a placement method that (1) combines length calculations to **obtain an estimate** of the total interconnect-line length needed for connecting the circuit elements of the nets during a routing operation, and then (2) uses the combined length calculation

to identify a placement of the circuit modules. Kikuchi does not disclose, teach, or even suggest such a method.

Accordingly, Applicants respectfully submit that Kikuchi does not render claim 61 unpatentable. As Claims 62-64 are dependent on claim 61, Applicants respectfully submit that claims 62-64 are patentable over Kikuchi for at least the same reasons that were discussed above for claim 61.

In view of the foregoing, Applicants respectfully request reconsideration and withdrawal of the § 102 rejection of claims 61-64.

V. Rejection of claims 88-96 under § 102(e)

Claims 88-96 were rejected under § 102(e) as being unpatentable over Kikuchi. Claims 89-96 are dependent directly or indirectly on independent claim 88. Claim 88 recites a method that places circuit modules in an integrated circuit ("IC") layout. The IC layout includes a set of circuit elements. The method identifies a connection graph that connects the set of circuit elements. The connection graph has a plurality of edges. At least two of the edges are neither parallel nor orthogonal to each other. The method identifies a placement metric based on the connection graph. The method uses the placement metric to identify a placement of the circuit modules.

Applicants respectfully submit that Kikuchi does not disclose, teach, or even suggest such a method. For instance, Applicants respectfully submit that Kikuchi does not disclose, teach or even suggest a method that:

- identifies a connection graph that connects the set of circuit elements, where the connection graph has a plurality of edges and where at least two of the edges are neither parallel nor orthogonal to each other;
- identifies a placement metric based on the connection graph; and
- uses the placement metric to identify a placement of circuit modules.

The Examiner rejects claim 88 on the basis of being similar manner as claim 4. As discussed above, Kikuchi describes a method that obtains a distance between two components in order to determine the capacity between the edges of the components. In contrast, claim 88 recites in part, a placement method that (1) **identifies a placement metric** based on a connection graph, and (2) uses the placement metric to identify a placement of the circuit modules. Nowhere in Kikuchi are such limitations disclosed, taught or even suggested.

Accordingly, Applicants respectfully submit that Kikuchi does not render claim 88 unpatentable. As claims 89-96 are dependent on claim 88, Applicants respectfully submit that claims 89-96 are patentable over Kikuchi for at least the same reasons that were discussed above for claim 88.

In view of the foregoing, Applicants respectfully request reconsideration and withdrawal of the § 102(e) rejection of claims 88-96.

V. Allowable claims 11, 46- 47 and 50

Claims 11, 46-47, 50 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants thank the Examiner for the finding of allowability of these claims. However, Applicants respectfully submit that the base independent claims of these allowed claims is also allowable in view of the remarks mentioned above.

VI. Information Disclosure Statement

In the Office Action, the Examiner indicated that the foreign patent documents (cite no.45-51) and non-patent documents (cite no.52-88) cited in the Information Disclosure Statements dated December 8, 2003 needed to be supplied for the Examiner's consideration. Applicants respectfully submit that these IDS's have been received by the Patent Office. *See* attached copies of the return receipt postcard sent along with the IDS's filed 12/08/2003, which indicate 12/10/2003 and 12/11/2003 as the received dates for the IDS's; *see also* attached copy of the PAIR system report showing that the Patent Office received these references. The PAIR system also shows many of the references cited in the IDS's as being electronically scanned into the PAIR system. Notwithstanding, in the next week, Applicants will review the PAIR system and will contact the Examiner and the Patent Office to ensure that these references have been received by the Patent Office. If any references appear missing at that time, Applicants will resubmit these references for the Examiner's review.

CONCLUSION

In view of the foregoing, it is submitted that all pending claims, namely claims 4-13, 43-64, 88-96 are in condition for allowance. Reconsideration of the rejections and objections is requested. Allowance is earnestly solicited at the earliest possible date.

Respectfully submitted,

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Serial/Patent No.: 09/731,891 Atty/Secty: Ma/ka
Filing Date: 12/6/00 Date Mailed: 12/8/2003
Atty Docket: SPLX.P0002
Applicant(s): Steven Teig

TITLE: **Method and Apparatus for Considering Diagonal Wiring in Placement**

The following has been received by the U.S. Patent & Trademark Office on the date stamped hereon:

1. Transmittal Form
2. Information Disclosure Statement (2 pages)
3. Form PTO-1449 (4 pages)
4. 46 cited references

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PATENT APPLICATION INFORMATION RETRIEVAL

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Search results as of: 8-3-2004::17:41

Search results for application number:09/731,891			
Application Number:	09/731,891	Customer Number:	23349
Filing or 371(c) Date:	12-06-2000	Status:	Non Final Act Mailed
Application Type:	Utility	Status Date:	03-02-2004
Examiner Name:	DO, THUAN V	Location:	ELECTRONIC
Group Art Unit:	2825	Location Date:	-
Confirmation Number:	1036	Earliest Publication No:	US 2002-013
Attorney Docket Number:	SPLX.P0002	Earliest Publication Date:	09-19-2002
Class/ Sub-Class:	716/010	Patent Number:	-
First Named Inventor:	Steven Teig, Menlo Park, CA	Issue Date of Patent:	-
Title Of Invention:	Method and apparatus for considering diagonal wiring in placement		

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File History

Date	Contents Description
03-03-2004	Mail Non-Final Rejection
02-20-2004	Non-Final Rejection
12-11-2003	Reference capture on IDS
12-10-2003	Reference capture on IDS
01-10-2004	IFW Amended case processing Complete
12-11-2003	Information Disclosure Statement (IDS) Filed
01-10-2004	Date Forwarded to Examiner
01-10-2004	Date Forwarded to Examiner
12-11-2003	Request for Continued Examination (RCE)
01-10-2004	Express Abandonment (for Entry of CPA / RCE / Rule129)
12-11-2003	Request for Extension of Time - Granted
12-10-2003	Information Disclosure Statement (IDS) Filed
12-11-2003	Workflow - Request for RCE - Begin
07-07-2003	Mail Final Rejection (PTOL - 326)
07-02-2003	Petition Decision - Granted

02-13-2002	Rescind Nonpublication Request for Pre Grant Publication
06-11-2003	Final Rejection
06-06-2003	Petition Entered
04-30-2003	Date Forwarded to Examiner
03-12-2003	Response after Non-Final Action
03-12-2003	Request for Extension of Time - Granted
03-07-2003	Information Disclosure Statement (IDS) Filed
11-06-2002	Mail Non-Final Rejection
11-04-2002	Non-Final Rejection
08-08-2002	Case Docketed to Examiner in GAU
02-13-2002	Rescind Nonpublication Request for Pre Grant Publication
04-27-2001	New or Additional Drawing Filed
04-27-2001	Incoming Letter Pertaining to the Drawings
06-07-2001	Case Docketed to Examiner in GAU
05-10-2001	Application Dispatched from OIPE
01-23-2001	Application Is Now Complete
01-23-2001	Notice Mailed--Application Incomplete--Filing Date Assigned
01-22-2001	Correspondence Address Change
01-05-2001	IFW Scan & PACR Auto Security Review
12-06-2000	Initial Exam Team nn